AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An input/output data pipeline circuit of a semiconductor memory device, comprising:

a control signal generating unit adapted to receive a clock signal and adapted to output a control signal, a first switching signal, and a second switching signal, according to a frequency of the clock signal;

a first transmitting unit adapted to receive data stored in a memory cell and to transmit data to an input/output driver in response to activation of the first switching signal and the second switching signal; and

a second transmitting unit adapted to transmit data to the input/output driver in response to activation of the control signal,

wherein the first transmitting unit and the second transmitting unit are adapted to be alternatively activated.

2. (Currently Amended) The input/output data pipeline circuit of claim 1, wherein the first transmitting unit comprises:

a first switching circuit adapted to output data in response to activation of the first switching signal;

a latching circuit ~~adaptred~~ adapted to latch and output the output of the first switching circuit; and

a second switching circuit adapted to output the output of the latching circuit to the input/output driver in response to activation of the second switching signal.

3. (Original) The input/output data pipeline circuit of claim 1, wherein the second transmitting unit comprises a third switching circuit, which is adapted to output data to the input/output driver in response to activation of the control signal.

4. (Original) The input/output data pipeline circuit of claim 1, wherein the first transmitting unit is adapted to be activated when the first switching signal and the second switching signal are activated, and the control signal is deactivated.

5. (Original) The input/output data pipeline circuit of claim 4, wherein the first switching signal is activated prior to activation of the second switching signal.

6. (Original) The input/output data pipeline circuit of claim 1, wherein the second transmitting unit is adapted to be activated when the control signal is activated, and the first and second switching signals are deactivated.

7. (Currently Amended) A semiconductor memory device comprising:

a memory cell core, which includes a plurality of memory cells;

an input/output driver adapted to receive first data from outside of the semiconductor memory device, in synchronization with a first clock signal, and adapted to output second data stored in the memory cell core, in synchronization with a second clock signal;

an input/output data pipeline circuit, which is connected to the memory cell core and the input/output driver, ~~wheih~~ which is adapted to transmit the second data stored in the memory cell core to the input/output driver, and which is adapted to transmit the first data received from outside of the semiconductor memory device to the memory cell core; and

a control signal generating unit, which is adapted to receive the first clock signal and the second clock signal, and which is adapted to output a control signal corresponding to frequencies of the first clock signal and the second clock signal,

wherein the input/output data pipeline circuit includes a first transmitting unit, which ~~which~~ is adapted to perform a transmission operation between the memory cell core and the input/output driver in response to activation of a first switching signal and a second switching signal, and a second transmitting unit which ~~which~~ is adapted to perform a transmission operation between the memory cell core and the input/output driver in response to activation of the control signal, and

wherein the first transmitting unit and the second transmitting unit are ~~apated~~ adapted to be alternatively activated.

8. (Original) The semiconductor memory device of claim 7, wherein the control signal generating unit which is adapted to detect a phase difference between the first clock signal and the second clock signal, and which is adapted to output the control signal with a logic state based on a detected result.

9. (Currently Amended) The semiconductor memory device of claim 7, wherein the first transmitting unit comprises:

a first switching circuit, which is which is adapted to be switched on and output the first data or the second data in response to activation of the first switching signal;

a latching circuit, which ~~which~~ is adapted to latch and output the output of the first switching circuit; and

a second switching circuit, which is which is adapted to be switched on and output the output of the latching circuit to the input/output driver in response to activation of the second switching signal.

10. (Original) The semiconductor memory device of claim 9, wherein the first transmitting unit is adapted to be activated when the first switching signal and the second switching signal are activated, and the control signal is deactivated.

11. (Original) The semiconductor memory device of claim 10, wherein the first switching signal is activated prior to activation of the second switching signal.

12. (Original) The semiconductor memory device of claim 9, wherein the second transmitting unit is adapted to be activated when the control signal is activated, and the first and second switching signals are deactivated.

13. (Original) The semiconductor memory device of claim 7, wherein the control signal generating unit is further adapted to receive information about operation modes of the semiconductor memory device, and the control signal corresponds to the first clock signal, the second clock signal, and information about operation modes of the semiconductor memory device.

14. (Original) The semiconductor memory device of claim 13, wherein when information about the operation modes of the semiconductor memory device indicates that the semiconductor memory device operates at a low frequency, the first switching signal and the second switching signal are activated, i.e., enter a predetermined logic state, the control signal is deactivated, and the first switching signal is activated prior to activation of the second switching signal.

15. (Original) A semiconductor memory device comprising:

a memory cell core, which includes a plurality of memory cells;

an input/output driver;

a control signal generating unit adapted to receive a first clock signal, a second clock signal, and information about operation modes of the semiconductor memory device, and which is adapted to output a first switching signal, a second switching signal, and a control signal corresponding to the first clock signal, the second clock signal, and information about the operation modes of the semiconductor memory device; and

an input/output data pipeline circuit, which is connected to the memory cell core and the input/output driver, and which is adapted to transmit data stored in the memory cell core to the input/output driver in response to activation of the first switching signal, the second switching signal, and the control signal,

wherein the input/output data pipeline circuit includes a first transmitting unit, which is adapted to be activated in response to activation of the first switching signal and the second switching signal, and a second transmitting unit which is adapted to be activated in response to activation of the control signal, and

wherein the first transmitting unit and the second transmitting unit are adapted to be alternatively activated.

16. (Original) The semiconductor memory device of claim 15, wherein the control signal generating unit is adapted to detect a phase difference between the first clock signal and the second clock signal, and is adapted to output the control signal with a logic state corresponding to a detected result, and if the control signal generating unit receives information about the operation modes of the semiconductor memory device indicating that the semiconductor memory device operates at a low frequency, the first transmitting unit is activated irrespective of the phase difference between the first clock signal and the second clock signal.